REMARKS

This Preliminary Amendment is being filed concurrent with the Divisional Patent Application filed on even date herewith. With this Preliminary Amendment claims 1-36 have been canceled without prejudice and claims 37-48 have been added. Claims 37-48 remain pending in the application and are presented for consideration and allowance.

The Specification has been amended at page 15 to provide a clerical correction to the specification. These changes were made in the parent application. Applicant respectfully requests consideration and approval of these changes to the Specification.

Attached hereto is a marked-up version of the changes made to the specification by the current Preliminary Amendment. The attached pages are captioned **"VERSION WITH MARKINGS TO SHOW CHANGES MADE".**

Any inquiry regarding this Preliminary Amendment should be directed to either Patrick G. Billig at Telephone No. (612) 573-2003, Facsimile NO. (612) 573-2005 or Kevin B. Sullivan at Telephone No. (858) 655-5228, Facsimile No. (858) 655-5859. In addition, all correspondence should continue to be directed to the following address:

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I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" services under 37 C.F.R. 1.10 on the date indicated above and is addressed to the Assistant Commissioner of Patents and Trademarks, Washington, D.C. 20231.

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VERSION WITH MARKINGS
TO SHOW CHANGES MADE

#3/B CC 12/10/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jong Chan	Examiner: Unknown
Serial No.:	Unknown (Parent Serial No.: 09/085,204)	Group Art Unit: Unknown
Filed:	Herewith (Parent Filing Date: May 27, 1998)	Docket No.: 10980422-3
Title:	MEMORY CONTROLLER SUPPORTING REDUNDANT SYNCHRONOUS MEMORIES	

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir/Madam:

This Preliminary Amendment is filed concurrent with the Divisional Patent Application filed on even date herewith. Please amend the above-identified application as follows:

IN THE SPECIFICATION

Please replace the paragraph beginning at page 15, line 7, with the following rewritten paragraph:

Fig. 6 illustrates the memory bus 230 and bus switches ~~288,~~ 290, 292, and 294 in each I/O control logic unit 212. Each memory bus 230 is composed of a number of signal paths (i.e., lines or traces) that carry address, data, and control signals. The address signals 266 are generated by the memory controller 224. The data signals 225 are received from the PCI bus 228. The control signals includes a local memory select signal 262, a remote memory select signal 264, and a read/write control signal 268A.

IN THE CLAIMS

Please cancel claims 1-36 without prejudice.

Please add new claims 37-48 as follows:

37. A method for controlling a transfer of data between a data processor and a data unit, the method comprising:

providing a plurality of control units, each control unit having a capability to control the transfer of data between the data processor and the data unit, each control unit having a memory device and signal paths coupled to the memory device, the signal paths enabling access to the associated memory device;

selecting one of the control units as a master control unit to control the transfer of data between the data processor and the data unit;

designating a second one of the control units as a slave control unit;

transferring the data between the data processor and the data unit by employing the memory device in the master control unit; and

synchronizing the memory device in the master control unit with the memory device in the slave control unit, the synchronizing including:

generating, in the master control unit, values for the signal paths associated with the master memory device to transfer data to the master memory device;

transferring a subset of the generated signal paths to the signal paths associated with the slave memory device; and

allowing the generated signals to perform the data transfer to the master memory device and the slave memory device.

38. The method of claim 37, wherein the generating step further comprises:

generating, in the master control unit, values for the signal paths associated with the slave memory device that enables access to the slave memory device.

39. The method of claim 37, further comprising:

associating an address and control signal path with each memory device that enables access to the corresponding memory device;

the generating step further comprising:

producing values for the address and control signal paths associated with the master memory device; and

the transferring step further comprising:

transmitting the address and control signal paths associated with the master memory device to the address and control signal paths associated with the slave memory device.

40. The method of claim 39, further comprising:

associating with the master memory device a first control signal that controls access to the slave memory device;

associating with each memory device a second control signal that controls access to the corresponding memory device;

the generating step further comprising:

producing values for the first control signal and the second control signal associated with the master memory device; and

the transferring step further comprising:

transmitting the first control signal associated with the master memory device to the second control signal associated with the slave memory device.

41. The method of claim 39, further comprising:

associating with each control unit a data signal path; and

the transferring step further comprising:

receiving data values for the data signal path associated with the master memory device; and

transmitting the received data values to the data signal path associated with the ~~salve~~ slave memory device.

42. The method of claim 37, further comprising:

associating with the signal paths associated with each memory device a control mechanism that enables a transfer of values from a first signal path to a second signal path; and

enabling the control mechanism associated with the master memory device and the control mechanism associated with the slave memory device to transfer values between the master signal paths and the slave signal paths.

43. The method of 42, further comprising:

disabling the control mechanism associated with a memory device to inhibit a transfer and receipt of signal paths values.

44. The method of claim 37, further comprising:

suspending the master control unit from controlling the data transfer between the data processor and the data unit;

enabling the ~~salve~~ slave control unit to control the transfer of data between the data processor and the data unit; and

transferring the data between the data processor and the data unit by employing the memory device in the slave control unit.

45. The method of claim 44, wherein the suspending step further comprises:

determining that the master control unit has experienced an operational failure.

46. The method of claim 45, wherein the determining step further comprises:

receiving an indication that the memory device in the master control unit has failed.

47. The method of claim 37, further comprising:

disabling the master control unit from accessing the slave memory device; and

suspending operation of the slave control unit.

48. The method of claim 37, wherein the disabling step further comprises:

determining that the slave control unit has experienced an operational failure.